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Author Poan Tsai
Author's Email Address No Public.
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Abstract
Continuous advancements in the field of very large scale integrated circuits and very high speed integrated circuits have resulted in smaller chip sizes, smaller device geometries, and millions of closely spaced interconnections in one or more levels that connect the various components on the chip. Due to steady decrease in chip area and increase in clock frequencies, the influence of interconnects parasitic on circuit behavior becomes significant. In this study, we focus on modeling improvement for RLC crosstalk and parasitic capacitance.
In the past, most existing noise models only consider capacitive coupling. However, at current operating frequencies, inductive crosstalk effects should be included for complete coupling noise analysis. One aspect of on-chip inductance that has not been studied well is mutual inductive coupling. Mutual inductance causes signal integrity issues by injecting noise pulses on a victim line. The injected noise can either cause functional failure or change the delay of the victim line. Based on transmission line theory, we propose a simple RLC crosstalk model. Due to its simplicity, the model is useful in understanding noise waveform shapes due to capacitive and inductive coupling and also their dependencies on various parameters. The proposed model will be particularly useful in investigating the effect of physical design changes (linewidth, spacing, etc.) on noise.
Furthermore, based on 2D simulation result, we show that magnitude of slope regarding non-planar interconnects will affect the parasitic capacitance of crossover interconnects, which is ignored by previous investigations. To precisely predict the capacitances of the 2D interconnect, the sloping issue should be accounted for.
Advisory Committee T. K. Chiang - advisor

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